WEST Search History

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DATE: Friday, April 08, 2005

Hide?	Set Name	Query	Hit Count
		DB=PGPB,USPT; PLUR=NO; OP=ADJ	
☐	L83	(cpu or processor) with L82	5
☐	L82	L14 with (fpga or pld)	70
☐	L81	cpu with L79	12
☐	L80	processor with L79	33
☐	L79	L14 with (programmable gate$1 or programmable logic)	210
☐	L78	L77 not (L65 or L63 or L61 or L60 or L58 or L70 or L75)	270
☐	L77	processor with L74	324
☐	L76	L75 not (L65 or L63 or L61 or L60 or L58 or L70)	6
☐	L75	cpu same L74	43
☐	L74	L15 with (programmable gate$1 or programmable logic)	1486
☐	L73	L70 not (L65 or L63 or L61 or L60 or L58)	18
☐	L72	L70 not L58	18
☐	L71	L70 not L60	20
☐	L70	cpu same L69	26
☐	L69	L15 with (fpga or pld)	718
☐	L68	L15 same (fpga or pld)	1488
		DB=USPT,USOC; PLUR=NO; OP=ADJ	
☐	L67	L66 not (L65 or L63 or L61 or L60 or L58)	44
☐	L66	processor with L59	94
☐	L65	processor with L62	50
☐	L64	processor same L62	86
☐	L63	core same L62	17
☐	L62	L15 with (fpga or pld)	168
☐	L61	L60 not L58	17
☐	L60	cpu same L59	23
☐	L59	L15 with (programmable gate$1 or programmable logic)	460
☐	L58	cpu same L57	18
☐	L57	L15 same (fpga or pld)	383
☐	L56	cpu and L55	386
☐	L55	L15 and (fpga or pld)	1104
☐	L54	logic integrated circuit$1 and L22	0
☐	L53	L22 and (programmable gate$1 or programmable logic)	0

☐	L52	L22 and (fpga or pld)	0
☐	L51	enabl$3 and (L2 or L6)	2
☐	L50	enabl$3 and L49	1
☐	L49	(L2 or L6) and programmable	1
☐	L48	(L2 or L6) and logic	2
☐	L47	L2 or L6 and logic	2
☐	L46	cpu with L44	4
☐	L45	reprogram$4 with L44	4
☐	L44	fpga with (simulat$3 or emulat$3)	312
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=NO; OP=ADJ		
☐	L43	reprogram$4 with L42	0
☐	L42	fpga with (simulat$3 or emulat$3)	86
☐	L41	fpga simulator	0
	DB=USPT; PLUR=NO; OP=ADJ		
☐	L40	US-6260172-B1.did.	1
☐	L39	US-6089460-A.did.	1
☐	L38	US-6260172-B1.did.	1
	DB=PGPB; PLUR=NO; OP=ADJ		
☐	L37	US-20010011214-A1.did.	1
☐	L36	US-20010011214-A1.did.	1
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=NO; OP=ADJ		
☐	L35	cpu and L34	12
☐	L34	logic integrated circuit$1	925
	DB=PGPB,USPT; PLUR=NO; OP=ADJ		
☐	L33	5968161.uref.	6
☐	L32	altera.as. and L31	1
☐	L31	fpga same cpu	1275
☐	L30	altera.as. and cpu	197
	DB=USPT; PLUR=NO; OP=ADJ		
☐	L29	cpu and L27	40
☐	L28	cpu core$1 and L27	1
☐	L27	L26 and L15	129
☐	L26	L12.ti,ab,clm.	1510
☐	L25	5933642.pn.	1
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=NO; OP=ADJ		
☐	L24	5933642.pn.	1
☐	L23	L20 and L22	2
☐	L22	firmware or nanoinstruction$1 or nano-instruction$1 or nanocode or nano-code or nanoprogram or nano-program or L21	16037
☐	L21	microinstruction$1 or micro-instruction$1 or microcode or micro-code or micro-operation$1 or microoperation$1 or micro-op$1 or microop$1 or micro-program$1 or microprogram$1	11247

☐	L20	cpu and L19	222
☐	L19	field programmable gate array$1 or fpga$1	3520
	DB=PGPB,USPT; PLUR=NO; OP=ADJ		
☐	L18	cpu core$1 and L17	12
☐	L17	L12 same L15	1753
☐	L16	L13 and L15	98
	DB=USPT,PGPB; PLUR=NO; OP=ADJ		
☐	L15	firmware or nanoinstruction$1 or nano-instruction$1 or nanocode or nano-code or nanoprogram or nano-program or L14	58062
☐	L14	microinstruction$1 or micro-instruction$1 or microcode or micro-code or micro-operation$1 or microoperation$1 or micro-op$1 or microop$1 or micro-program$1 or microprogram$1	14972
	DB=PGPB,USPT; PLUR=NO; OP=ADJ		
☐	L13	cpu core$1 and L12	150
☐	L12	field programmable gate array$1 or fpga$1	18399
☐	L11	L9 and core	3138
☐	L10	(L2 or L6) and L9	0
☐	L9	field programmable gate array$1	14226
☐	L8	(L2 or L6) and fpga	0
☐	L7	(L2 or L6) and core	0
☐	L6	5675777.pn.	1
☐	L5	glickman.in. and jeff.in.	8
☐	L4	glickman.in. and taraplex.as.	0
☐	L3	glickman.in. and teraplex.as.	0
☐	L2	6389528.pn.	1
☐	L1	pappalardo.in. and tesi.in.	7

END OF SEARCH HISTORY